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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/563,415	01/03/2006	Kees Marinus Maria Van Kaam	NL03 0806 US1	4525

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2117	

NOTIFICATION DATE	DELIVERY MODE
08/13/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/563,415	VAN KAAM, KEES MARINUS MARIA	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 January 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a FINAL Office Action in response to the AMENDMENT, filed 7/8/2008.

Claims 1-24 were previously rejected. Claims 25-29 are new.

Claims 1-29 are pending.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file, for EUROPEAN PATENT OFFICE (EPO) Application No. 03102062.1, filed 07/09/2003.

The U.S. Application No. 10,563415, filed 01/03/2006, is a national stage entry of PCT/IB04/51089, International Filing Date: 07/01/2004.

The drawings of the Replacement Sheet for Fig. 1, received on 7/8/2008 are acceptable. Therefore, the objection to the drawings, with respect to Fig. 1, has been withdrawn in view of the amendment.

Objection to the Claims has been withdrawn in view of the amendment to the claims.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because the "voltage controller" and "clock controller" described in the specification are designated as "Controlled voltage" and "Controlled frequency" with the corresponding reference characters in Figs. 2-4. The drawings should be changed accordingly to be consistent with the description in the specification.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended

replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims1-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Schwarz (US Patent No. 6,496,947) issued December 17, 2002.

Regarding independent Claims 1, 20 and 23, Schwarz discloses a semiconductor device (integrated circuit 10) and a method for testing the integrated circuit, Figs. 1, 5 and 6, comprising:

A functional device (Memory array 12) responsive to test stimuli, using a test algorithm sequences through each address location of memory array 12 for performing several write and read operations at each location. For example, the test algorithm can

initially write a test pattern to memory array 12 such that each memory cell has a definite state. The test algorithm then reads the stored data from each memory cell, writes the opposite state to the memory cell and then reads the stored opposite state from the memory cell.

an integral characterization unit (BIST) circuit 18 including test address output 60, test data and control output 61, expected data output 62, error input 63, wait output 64, repair output 65, overflow input 66, mode input 67 and test enable input 68, the BIST is operable to control the memory array 12 in response to test enable input 40 and field/factory mode input 42, which are generated externally from a memory tester 252 coupled to integrated circuit 10. Memory tester 250 provides an adjustable system clock 254 and an adjustable supply voltage 256 to integrated circuit 10 for testing integrated circuit 10 under various operating conditions.

Regarding Claims 2-19, 22, 24-29, BIST circuit 18 controls outputs 60 and 61 to perform a sequence of writes and reads on memory array 12. The test algorithm sequences through each address location of memory array 12 and performs several write and read operations at each location. A compare circuit 28 compares the data that was read from the memory array with expected data provided by BIST circuit 18. If the data read from a particular cell or address of memory array 12 does not match the expected data, compare circuit 28 activates error output 90 to signal that the memory cell or location being tested is faulty.

In Fig. 5, the test algorithm may repeat the test procedure a number of times with various test patterns and in various orders through the address sequence to verify the

functionality of RAM 12. At step 302, memory tester 252 repeats the BIST test algorithm at various supply voltages and clock speeds.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques H. Louis-Jacques can be reached on (571) 272-4150. The fax

phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JAMES C KERVEROS/
Primary Examiner, Art Unit 2117

Date: 12 August 2008
Office Action: Final Rejection

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